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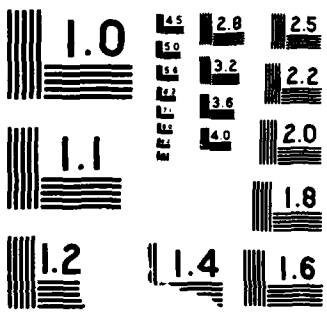
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N-channel Polysilicon-gate FETs have been fabricated in a laser-melted silicon-on-SiO_2-on-PLZT structure. Channel mobilities in the devices are 50 cm^2/Vs with threshold and source-to-drain breakdown voltages as expected from the dielectric thickness and channel doping used. PLZT wafers subjected to the same processing temperatures still show an excellent electro-optic effect.

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FABRICATION OF POLYSILICON GATE FET IN LASER MELTED SILICON ON SILICON DIOXIDE ON PLZT

Indexing terms: Field-effect transistors, Ferroelectric materials

N-channel polysilicon-gate FETs have been fabricated in a laser-melted silicon-on-SiO_2-on-PLZT structure. Channel mobilities in the devices are 50 cm^2/Vs with threshold and source-to-drain breakdown voltages as expected from the dielectric thickness and channel doping used. PLZT wafers subjected to the same processing temperatures st... show an excellent electro-optic effect.

Lanthanum-modified lead-zirconate-titanate PLZT or [(Pb, La) (ZR, Ti) (O_3)] is a ferroelectric ceramic material known for its strong quadratic electro-optic effect, excellent transparency and relative ease of fabrication. These properties make it suitable for various electro-optic device applications such as memories and spatial light modulators.[1] The fabrication of silicon semiconductor switches on an electro-optic substrate[2] such as PLZT enables the realisation of a completely integrated optical switch. We report here on the preparation of silicon films on PLZT and the subsequent laser melting and device fabrication in these films.

2 in (51 mm)-diameter PLZT wafers were purchased commercially. The polysilicon and SiO_2 films were deposited at 750 C in a horizontal reactor using silane, oxygen (if needed) and nitrogen gases all at atmospheric pressure. Wafers were first cleaned in a solution of hydrogen peroxide, ammonium hydroxide and deionised water (Standard Clean One or SC1), then rinsed in deionised water. 300 nm of SiO_2 was then deposited on the back side to protect the PLZT from the effect of subsequent acids (especially HF). Next, on the top side, a thick 3500 nm layer of SiO_2 was deposited, followed immediately by a 600 nm layer of polysilicon. The thick SiO_2 layer acted as a thermal buffer during the laser melting of the polysilicon.

Laser melting of the polysilicon layer was accomplished by using an argon ion laser in the TEM_{01} mode. The dwell time of the laser was controlled by using a spatial filter to reduce the spot size in the direction of scanning and appropriately adjusting the scanning speed. This reduced dwell time, coupled with thermal isolation of the PLZT substrate from the polysilicon by the thick SiO_2 layer, allowed the melting of the polysilicon without damaging the temperature-sensitive

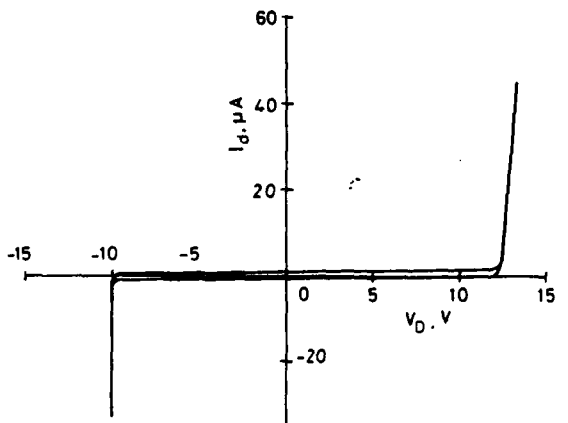

Fig. 1 *Source/drain characteristic of N-channel FET made on PLZT structure*

Gate voltage = −10 V

Fig. 1 shows a typical source/drain characteristic. The sharp 12 V breakdown is approximately what one expects from the channel implant (the bulk trailer wafers have a 15 V breakdown), indicating that high-quality recrystallised material has been achieved. Fig. 2 shows a family of curves of an FET on the PLZT structure. The threshold of 5·5 V is what one expects from the dielectric thickness and channel doping. The failure to reach saturation is accounted for by a high contact resistance. Mobility is measured in the linear region at low source-drain voltage and is approximately 50 cm^2/Vs.

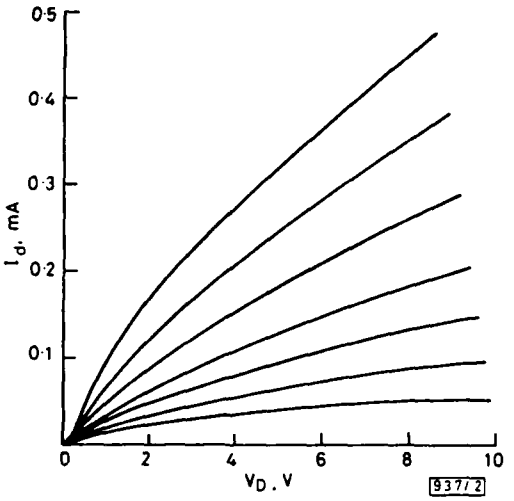

Fig. 2 *I/V characteristics of N-channel FET made on PLZT structure*

Offset = +8 V. There are eight steps at 2 V/step. $L = 4{\cdot}5\,\mu m$ and $W = 40\,\mu m$

In conclusion, it has been demonstrated that it is possible to make device-quality silicon films on PLZT. Devices in these films show MOSFET behaviour with good breakdown and threshold characteristics. The PLZT wafers subjected to the same high-temperature steps as the processed PLZT wafer show no degradation in electro-optic properties. Further work is now in progress to make electro-optic switches in this silicon/PLZT structure and demonstrate the viability of using these switches in spatial light modulators (SLMs).

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